Customer No.: 31561
Application No.: 10/711,536
Docket No.: 13301-US-PA

REMARKS

Claim Rejections Under U.S.C. 35 §102

The Office Action rejected claims 1 and 5-19 under 35 U.S.C. 102(e) as being anticipated by Farnworth et al. US Patent 6,908,794.

In response to the rejection to claims 1 and 5-19 under 35 U.S.C. 102(e) as being anticipated by Farnworth et al. US Patent 6,908,794, Applicants hereby otherwise traverses this rejection. As such, Applicant submits that claims 1 and 5-19 are in condition for allowance.

With respect to claim 1, as originally filed, recites in part:

A wafer level chip scale package structure process, comprising:

providing a **glass substrate** having a first surface and a second surface, wherein an interconnect pattern is disposed on the first surface of the glass substrate;

providing a wafer comprising a plurality of chips and having an active surface and a back surface, wherein a plurality of **bumps** is disposed on the active surface of the wafer;

flipping the wafer, so that the active surface of the wafer faces the first surface of the glass substrate;

disposing the wafer on the glass substrate and connecting the active surface of the wafer to the first surface of the glass substrate through attachment of the bumps and the interconnect pattern ... (Emphasis added.)

Applicant submits that such a wafer level chip scale package structure process as set forth in claim 1 is neither taught, disclosed, nor suggested by Farnworth et al. US Patent 6,908,794, or any of the other cited references, taken alone or in combination.

Farnworth teaches that "each die 10A includes a **semiconductor** substrate 14A containing integrated circuits" (FIG. 8A; Column 18, lines 3 and 4) (Emphasis added.). Therefore, it is submitted that Farnworth et al. US Patent 6,908,794 fails to teach, disclose or suggest a glass substrate, as set forth in claim 1. Further, Farnworth fails to teach "a plurality of bumps disposed on the active surface of the wafer". Furthermore, Farnworth fails to teach the steps of flipping the wafer and disposing the wafer on the glass substrate.

Accordingly, the present invention as set forth in claim 1 should not be considered as being anticipated by Farnworth, and thus claim 1 should be allowable.

Similarly, claim 10, as originally filed, recites in parts:

A wafer level chip scale package structure process, comprising:

providing a **glass substrate** having a first surface and a second surface;

providing a wafer comprising a plurality of chips that are to be separated along scribe-lines and having an active surface and a back surface, wherein a plurality **of pads** are disposed on the active surface of the wafer and cover a portion of the scribe-lines of the wafer;

flipping the wafer in order to face the active surface of the wafer to the first surface of the glass substrate and **attaching the active surface of the wafer to the first surface of the glass substrate** ... (Emphasis added.)

Applicant submits that such a wafer level chip scale package structure process as set forth in claim 10 is neither taught, disclosed, nor suggested by Farnworth et al. US Patent 6,908,794, or any of the other cited references, taken alone or in combination.

Because of the similar reasons addressed to claim 1, it is submitted that Farnworth et al. US Patent 6,908,794 fails to teach, disclose or suggest a glass substrate, as set forth in claim 10. Further, Farnworth fails to teach "a plurality of pads disposed on the active surface of the wafer and covering a portion of the scribe-line". Furthermore, Farnworth fails to teach the steps of "flipping the wafer and disposing the wafer on the glass substrate" and "attaching the active surface of the wafer to the first surface of the glass substrate".

If independent claim 1 is allowable over the prior art of record, then its dependent claims 2-9 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 1. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

If independent claim 10 is allowable over the prior art of record, then its dependent claims 11-19 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 10. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

The Office Action rejected claims 2-4 under 35 U.S.C. 102(e) as being unpatentable over Farnworth et al. US Patent 6,908,794 in view of Canning et al. US Patent 5,783,465.

With regard to the 103 rejections of claims by Farnworth in view of Canning, Applicants respectfully submit that these claims defined over the prior art references for at least the reasons discussed above.

Moreover, Canning's invention is not directed to a wafer-level packaging. Therefore, the motivation to combine Farnworth with Canning is thereby lacking. Withdrawal of the rejection is respectfully requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-19 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Belinda Lee

Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw